## CLAIMS

Amend the claims as follows.

1. – 49. (Canceled)

50. (New) A system comprising:

a plurality of multi-bit inputs;

a combinational stage configured to generate a plurality of partial products of the plurality of multi-bit inputs;

a hybrid summing module comprising one or more full adders, one or more half adders, and a plurality of registers;

where the hybrid summing module is configured to receive as inputs the plurality of partial products, and is configured to reduce the plurality of partial products to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders;

where outputs of each of the one or more full adders and outputs of each of the one or more half adders are coupled to inputs of respective ones of the plurality of registers; and

where any bits of the plurality of partial products that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders are coupled to inputs of respective ones of the plurality of registers.

51. (New) The system of claim 50, where the hybrid summing module further comprises a two-input adder, the two-input adder configured to receive the first partial summation and the second partial summation as inputs, and configured to produce a final summation.

52. (New) The system of claim 51, where the hybrid summing module is further configured to receive the final summation, and is further configured to reduce the final summation and the plurality of partial products to a first accumulated partial summation and a second aeeumulated partial summation via the one or more full adders and the one or more half adders.

53. (New) The system of claim 52, where bits of the final summation are coupled to inputs of respeetive ones of the plurality of registers.

54. (New) Thc system of claim 52, where the combinational stage and the hybrid summing module arc configured to implement a multiply-accumulate operation.

55. (New) The system of claim 50,

further comprising a summing module generator adapted to configure thc hybrid summing module to reduce the plurality of partial products; and

where the combinational stage, the hybrid summing module, and the summing module gencrator are parts of a single integrated circuit.

56. (New) Thc system of claim 55, where the summing module generator comprises one or more control elements.

57. (New) The system of claim 56, where the one or more eontrol elements are Combinational Logic Blocks (CLBs).

58. (New) The system of claim 56, where the one or more control elements are configured to implement the summing model generator as an application.

59. (New) The system of claim 55, where thc summing model generator is configured to generate the hybrid summing module.

60. (New) The system of claim 55, where the summing model generator is configured to dynamically reallocate resources of the single integrated circuit to implement the hybrid summing module.

61. (New) The system of claim 67,

where the single integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and

where the resources comprise at least some of the CLBs.

62. (New) The system of claim 67,

where the single integrated circuit comprises a plurality of Boolean function generators, the Boolean function generators comprising look-up tables (LUTs) to implement Boolean logic functions; and

where the resources comprise at least some of the plurality of Boolean function generators.

63. (New) The system of claim 67, where each of at least some of the LUTs are associated with ones of the plurality of registers.

64. (New) The system of claim 67, where the summing model generator is configured to enable at least some of the resources as the one or more full adders.

65. (New) The system of claim 67, where the summing model generator is configured to enable at least some of the resources as the one or more full adders, the one or more half adders, and the plurality of registers.

66. (New) The system of claim 65, where the summing model generator is configured to program an interconnection of the one or more full adders, the one or more half adders, and the plurality of registers to, at least in part, implement the hybrid summing module.

67. (New) The system of claim 55, where the summing model generator is configured to analyze a number of bits of equal significance among the plurality of partial products to determine, at least in part, a number of the one or more full adders, a number of the one or more half adders, and a number of the plurality of registers to implement the hybrid summing module.

68. (New) The system of claim 50,

further comprising a negater; and

where at least some of the plurality of partial products are configured to pass through the negater prior to being received as inputs of the hybrid summing module.

69. (New) The system of claim 68, where the combinational stage, the negater, and the hybrid summing module are configured to implement a real portion of a complex multiply operation.

70. (New) An integrated circuit comprising:

a hybrid summing module comprising one or more full adders, one or more half adders, and a plurality of registers,

where the hybrid summing module is configured to receive as inputs a plurality of multi-bit addends, and is configured to reduce the plurality of addends to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders,

where outputs of each of the one or more full adders and outputs of each of the one or more half adders are coupled to inputs of respective ones of the plurality of registers, and

where any bits of the plurality of addends that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders are coupled to inputs of respective ones of the plurality of registers; and

a summing module generator enabled to dynamically configure the hybrid summing module.

71. (New) The integrated circuit of claim 70, where the hybrid summing module further comprises a two-input adder, the two-input adder enabled to receive the first partial summation and the second partial summation as inputs, and configured to produce a final summation.

72. (New) The integrated circuit of claim 71, where the hybrid summing module is further enabled to receive the final summation, and is further configured to reduce the final summation and the plurality of addends to a first accumulated partial summation and a second accumulated partial summation via the one or more full adders and the one or more half adders.

73. (New) The integrated circuit of claim 72, where bits of the final summation are coupled to inputs of respective ones of the plurality of registers.

74. (New) The integrated circuit of claim 72, further comprising a combinational stage configured to generate the plurality of addends as partial produets of a plurality of multi-bit inputs.

75. (New) The integrated circuit of claim 74, where the combinational stage and the hybrid summing module are configured to implement a multiply-accumulate operation.

76. (New) The integrated circuit of claim 70, where the summing module generator comprises one or more control elements.

77. (New) The integrated circuit of claim 76, where the one or more control elements are Combinational Logic Blocks (CLBs).

78. (New) The integrated circuit of claim 70, where the summing model generator is enabled to generate the hybrid summing module.

79. (New) The integrated circuit of claim 70, where the summing model generator is enabled to dynamically reallocate resources of the integrated circuit to implement the hybrid summing module.

80. (New) The integrated circuit of claim 79,

where the integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and

where the resources comprise at least some of the CLBs.

81. (New) The integrated circuit of claim 79,

where the integrated circuit comprises a plurality of Boolean function generators, the Boolean function generators comprising look-up tables (LUTs) to implement Boolean logic functions; and

where the resources comprise at least some of the plurality of Boolean function generators.

82. (New) The integrated circuit of claim 79, where the summing model generator is configured to enable at least some of the resources as the one or more full adders.

83. (New) The integrated circuit of claim 79, where the summing model generator is configured to enable at least some of the resources as the one or more full adders, the one or more half adders, and the plurality of registers.

84. (New) The integrated circuit of claim 83, where the summing model generator is configured to program an interconnection of the one or more full adders, the one or more half adders, and the plurality of registers to, at least in part, implement the hybrid summing module.

85. (New) A method of designing a portion of an integrated circuit comprising:

identifying a plurality of multi-bit inputs;

instantiating a combinational stage in the integrated circuit, the combinational stage configured to generate a plurality of partial products of the plurality of multi-bit inputs;

instantiating a hybrid summing module in the integrated circuit, the hybrid summing module comprising one or more full adders, one or more half adders, and a plurality of registers;

connecting the plurality of partial products to the hybrid summing module as inputs;

configuring the hybrid summing module to reduce the plurality of partial products to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders;

where the configuring comprises coupling outputs of each of the one or more full adders and outputs of each of the one or more half adders to inputs of respective ones of the plurality of registers; and

where the configuring further comprises coupling any bits of the plurality of partial products that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders to inputs of respective ones of the plurality of registers.

86. (New) The method of claim 85,

further comprising instantiating a summing module generator in the integrated circuit; and

where the summing module generator is enabled to perform the configuring.

87. (New) The method of claim 86, where the integrated circuit is a Field Programmable Gate Array (FPGA).

88. (New) The method of claim 86, where the summing module generator is further enabled to perform the instantiating the hybrid summing module.

89. (New) The method of claim 85,

where the integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and

where the instantiating the hybrid summing module comprises implementing the one or more full adders using at least some of the CLBs.

90. (New) The method of claim 85,

where the hybrid summing module further comprises a two-input adder enabled to produce a final summation; and

where the configuring further comprises coupling inputs of the two-input adder to the first partial summation and the second partial summation.

91. (New) The method of claim 90, further comprising:

connecting the final summation to the hybrid summing module as an input; and

configuring the hybrid summing module to reduce the final summation and the plurality of partial products to a first accumulated partial summation and a second accumulated partial summation via the one or more full adders and the one or more half adders.

92. (New) The method of claim 91, where the combinational stage and the hybrid summing module are configured to implement a multiply-accumulate operation.

93. (New) A method of using an integrated circuit comprising:

implementing, via a summing module generator of the integrated circuit, a hybrid summing module on the integrated circuit; and

performing, using the hybrid summing module, a multiply operation.

94. (New) The method of claim 93, where the hybrid summing module comprises one or more full adders, one or more half adders, and a plurality of registers.

95. (New) The method of claim 94, where the implementing comprises configuring the hybrid summing module to reduce a plurality of multi-bit addends to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders.

96. (New) The method of claim 95, where the implementing further comprises coupling outputs of each of the one or more full adders and outputs of each of the one or more half adders to inputs of respective ones of the plurality of registers, and coupling any bits of the plurality of addends that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders to inputs of respective ones of the plurality of registers.

97. (New) The system of claim 95, where the implementing further comprises analyzing a number of bits of equal significance among the plurality of addends to determine, at least in part, a number of the one or more full adders, a number of the one or more half adders, and a number of the plurality of registers to implement the hybrid summing module.

98. (New) The method of claim 94,

where the integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and

where the implementing further comprises implementing the one or more full adders using at least some of the CLBs.

99. (New) The method of claim 93, where the implementing comprises dynamically reallocating resources of the integrated circuit to implement the hybrid summing module.